國立臺北大學電機工程學系專題報告

分數型頻率除頻器

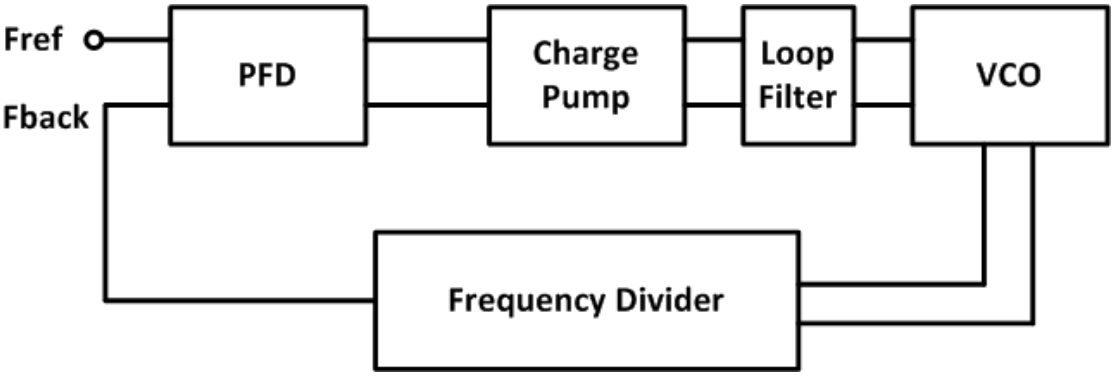
Frational Frequency Divider

組員：李易宸

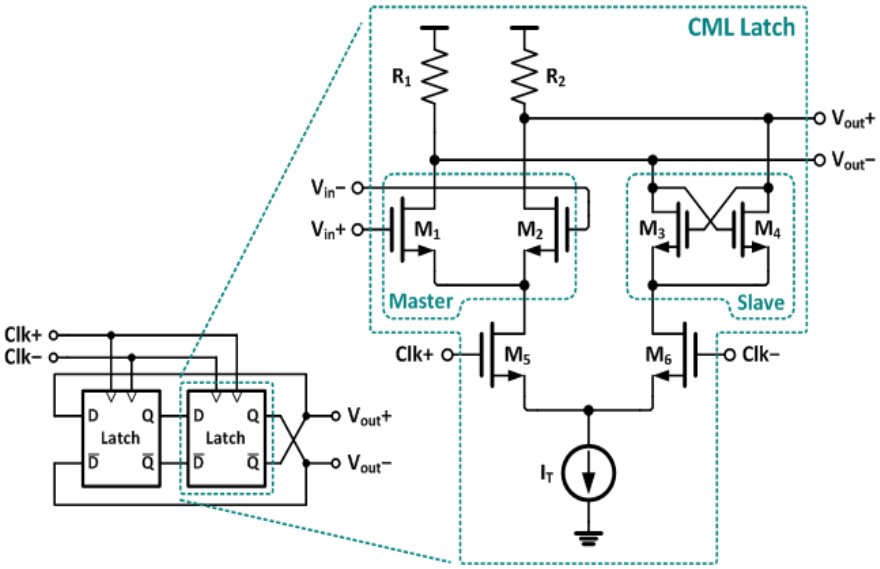
指導老師：郭岳芳 老師

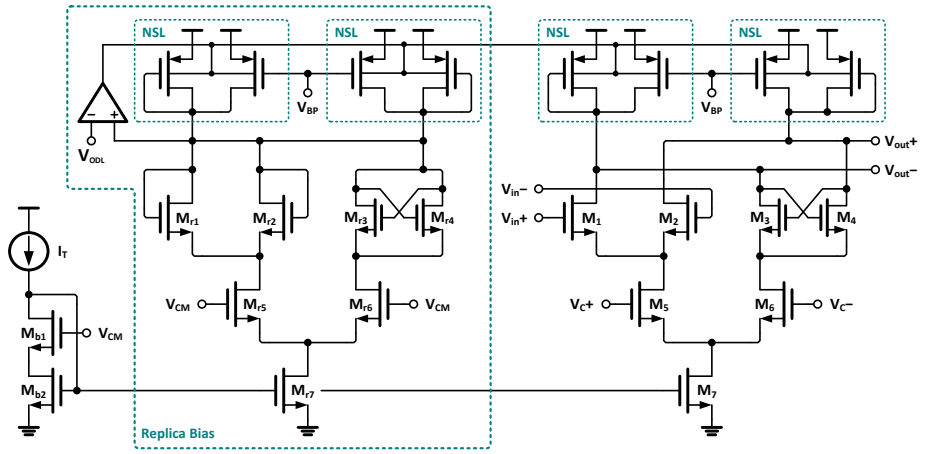
執行期間：104 年 7 月至 105 年 6 月

- **Related Technology of Frequency Divider**

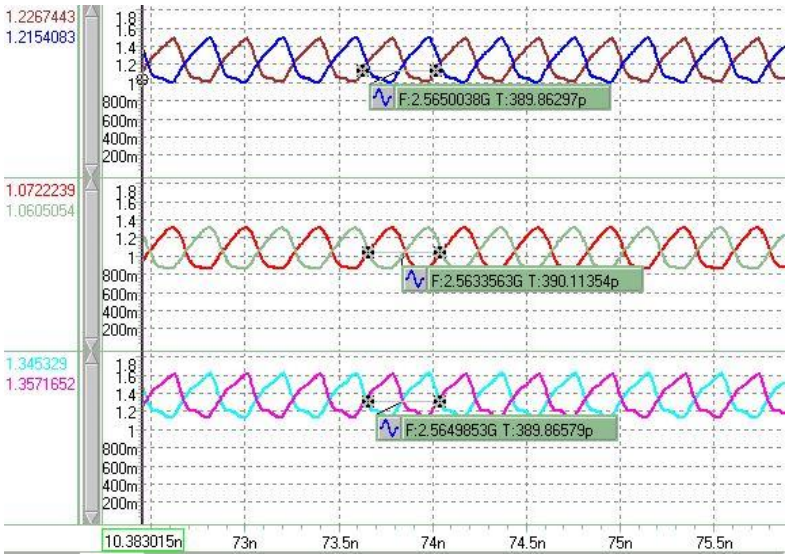


- **Differential High Speed Divider (Prescaler)**





- With BPC technique, self−resonate frequency of prescalers can be fixed, and so we can dramatically decrease the power consumption of prescaler.

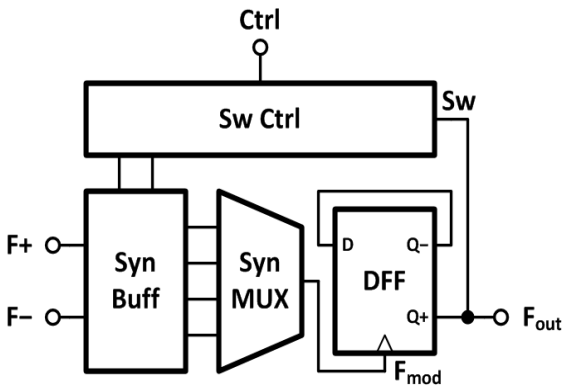


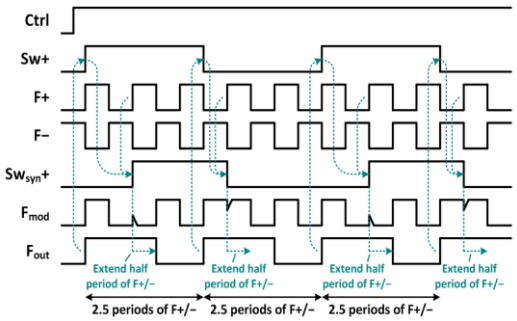
FF

TT

SS

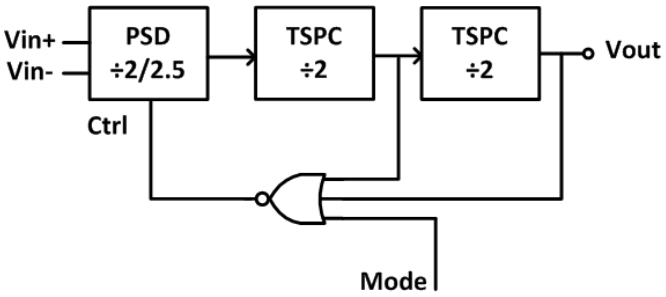
- **Operation of Phase Switch Divider**

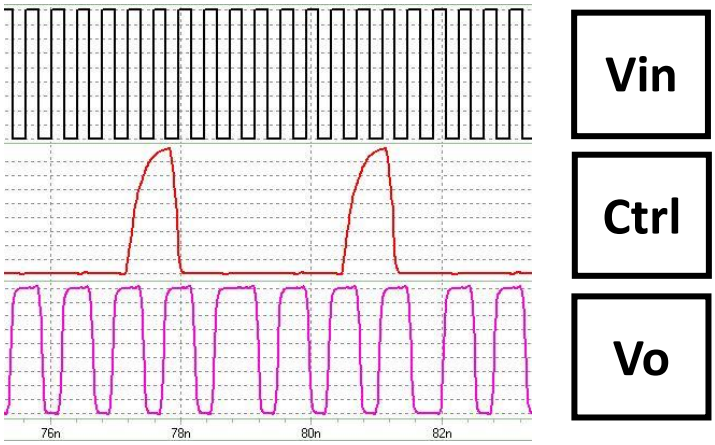




- When Ctrl = 0, PSD will perform function of modulus by 2
- When Ctrl = 1, PSD will perform function of modulus by 2.5
- Use TSPC for high speed operating.

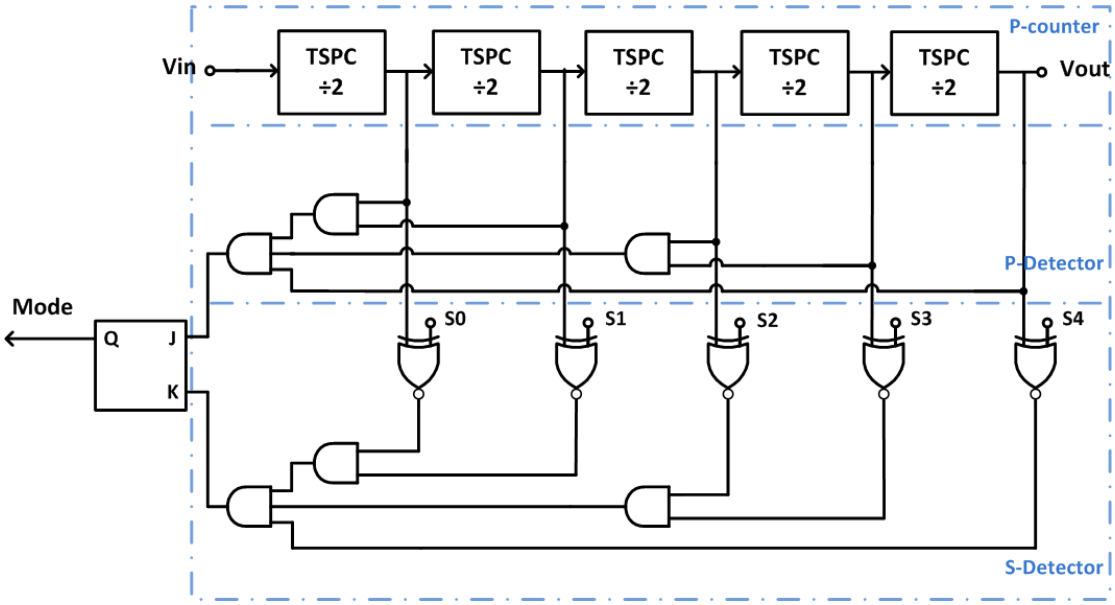
Fractional Dual-Modulus Prescaler (DMP)



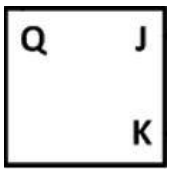


- Change the ‘’Ctrl‘’ signal to control the period.
- It will perform function of modulus by 8 or 8.5

Programmable Counter



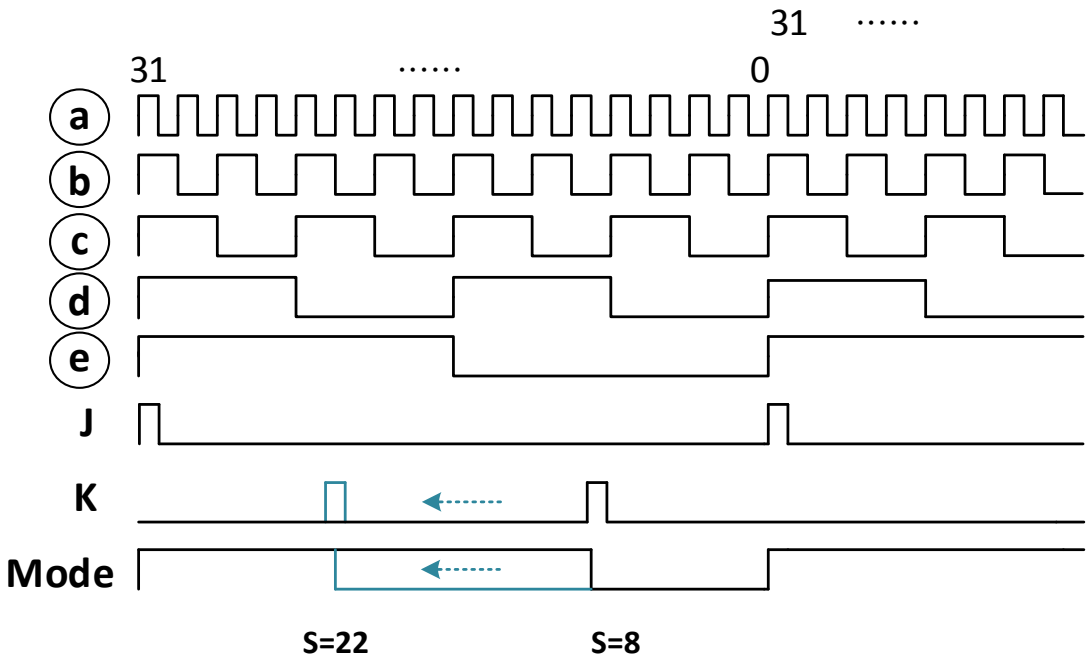
Operation of J K Flip-Flop

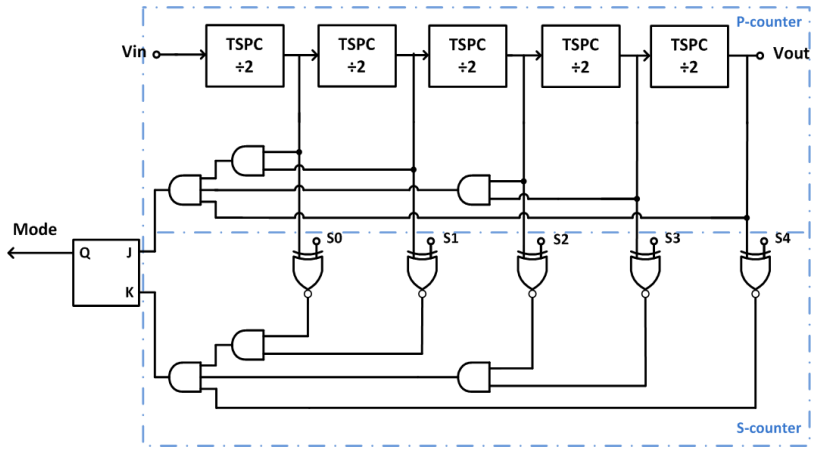


J	K	Q
0	0	Qn
1	0	1
0	1	0
1	1	Qn+1

- Avoid J=1,K=1
- When Mode=0, Dual-Modulus Prescaler will perform function of modulus by 8.5.

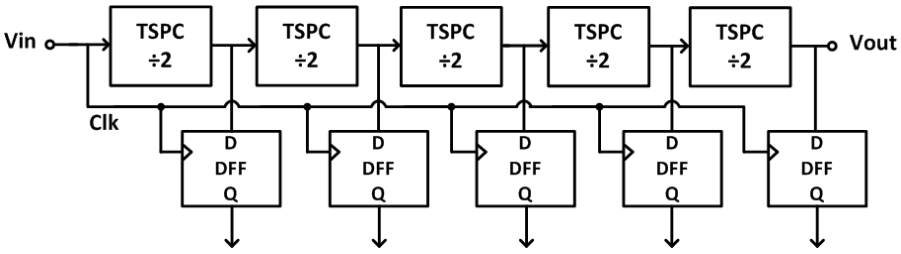
Operation of Programmable Counter





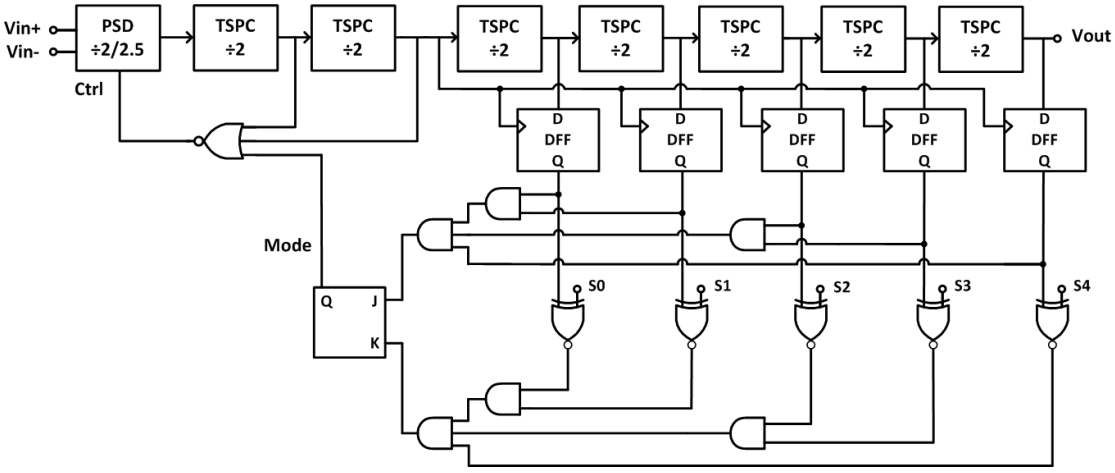
- Add ‘S’ Detector to control the ‘Mode’ signal.

Match the Signal of Programmable Counter



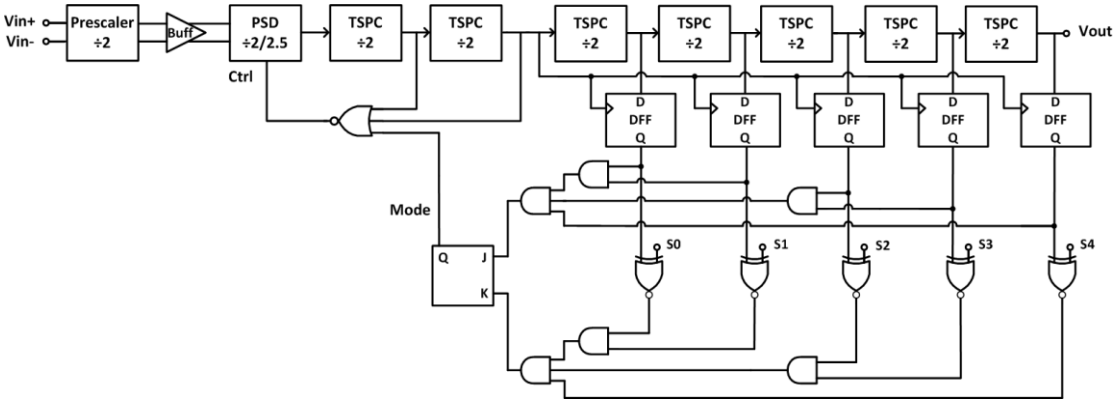
- Use D Flip-flop to match the signal to avoid glitch.

Range of Modulus of Fractional Divider



- Modulus=P*8+S*(0.5), for 5-bit P-counter and P/S Detector.
  → Modulus= 256.5~271.5 (in steps of 0.5)

Range of Modulus for Frequency Divider



- Modulus=2*(256.5~271.5) =513~543 (in steps of 1)
- Achieve operating frequency from 5.13 GHz to 5.43 GHz in steps of 10 MHz.

Comparison

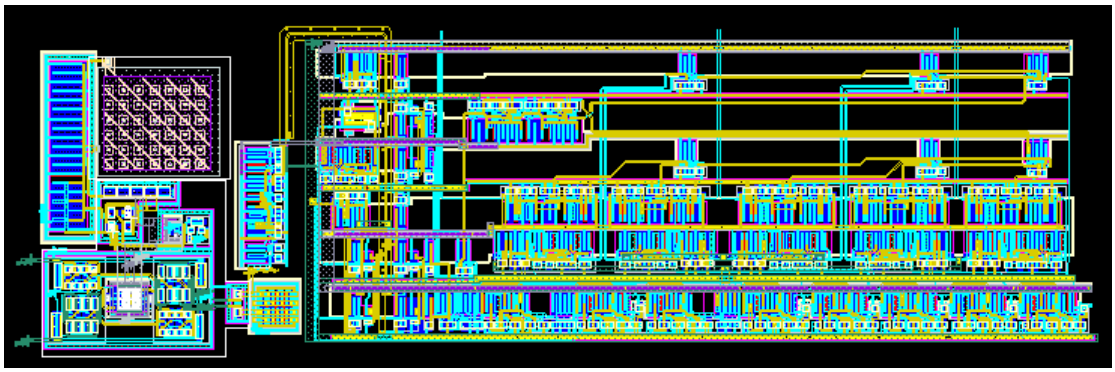
◆ Power Consumption

	Divider	**Buffer**	**Total**
Original Work	4.8mW	2.9mW	7.7mW
This Work	6.16mW*	1.64mW	7.8mW

◆ Performance

	Operating Frequency	**VCO Frequency Steps**	**Division Ratio**	**Fref**
Original Work	5.14~5.36 GHz 5.72~5.86 GHz	20 MHz	514~536 572~586	10 MHz
This Work	5.13~5.43 GHz	10 MHz	513~543	10 MHz

LAYOUT



Conclusion

- By Using Phase Switch Divider with TSPC Structure
  - Create a smaller division ratio's step of Frequency Divider.
  - Operating in Higher Frequency.
- By Using D Flip-Flops in Counter:
  - Perfect align the signal delivered to P-counter and S-counter.
  - Brings more power consumption and layout area.

Future Work

- Finish the whole Frequency Synthesiser
- Finish layout of Frequency Divider
- Reduce the current used in Prescaler to decrease the power consumption.
- Reduce the buffer used in Frequency Divider to decrease the power consumption.
- Change D Flip-Flops used in Counter to decrease the power consumption.

Reference

- [1] S.-I. Liu and C.-Y. Yang , "A Phase Locking Loop," *Tsang Hai*, 2006.
- [2] I.-A. Young, J.-K. Greason, J.-E. Smith, and K.-L.Wong, "A PLL Clock Generator with 5 to 110-MHz of Lock Range for Microprocessors," *in IEEE Int. Solid-State Circuit Conf. Dig. Tech. Papers*, pp. 50-51, 1992.
- [3] Y.-H. Chuang, S.-L. Jang, J.-F. Lee, and S.-H. Lee, "A Low Voltage 900-MHz Voltage Controlled Ring Oscillator With Wide Liming," *in IEEE Asia-Pacific Conf. on Circuits and Systems Tech. Papers*, pp. 301–304, 2004.
- [4] B. Razavi, "Design of Analog CMOS Integrated Circuits," *1ST ED., McGraw-Hill*, 2001.