High-Frequency Multi-Phase PLL with Process Compensation Scheme

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Abstract—**This work proposes a new structure of interpolating multiphase ring oscillator with high oscillation frequency. By optimizing a partial output interchanging scheme and using diagonally interpolating technique, 7.5GHz design without phase overlap is achieved in Phase Lock Loop (PLL). The design demonstrates improvements in oscillation frequency and phases of even stage of differential ring oscillator. Hspice circuit simulation and analysis confirms validity of such structure. This result overcomes the current 6GHz frequency limitation of .18 um process, without using any inductance component to reduce chip area.**

Index Terms—**multiphase ring oscillator, PLL, interpolating ring oscillator, high-speed clock recovery circuit**

I. INTRODUCTION

PLL can be used as clock generator in high-speed clock recovery circuit [2], DVD writer [3], etc. In all the sub-circuits of PLL, ring oscillator plays an indispensable role. Its oscillation frequency, phase number, tuning range, linearity, jitter, all of them affect whole of the PLL circuit. Currently, with the evolution of process technology, the highest oscillation frequency achievable is a major bottleneck in high speed multiphase applications.

Ring oscillator can be classified into three categories roughly. The first one is a single ended ring oscillator [4], which has good linearity and simple design. However, the highest oscillation frequency is inversely proportional to increasing number of stages and phases. A single ended ring oscillator can be realized in odd stages only and easily affected by chip manufactory process and signal noise. The second one is a LC ring oscillator [5]. Although it has higher oscillation frequency, it need more chip area to form inductances and has small tuning range. The third one is a differential ring oscillator [6]. It has better capabilities of anti-noise and gets more phases in the same oscillation frequency comparing to a single ended ring oscillator. It can reduce process error by Bulk-controlled Process Compensator (BPC). This work discusses many the third type of ring oscillator. In previous studies a two-stage differential ring oscillator [7] without interpolating scheme can realize any number of stages in ring oscillator. Oscillation frequency decreases with increasing number of stages. Another Eight-phase-output ring oscillator based on three-stage sub-feedback loops [8] which increases its oscillation frequency and doesn't be decreased while the stage number increases. It uses differential ICO delay cell to decrease the noise from VDD and GND. It gets low oscillation frequency because it interchanges inferior part of outputs of sub-feedback loops. Another 5×9 array oscillator [9] decrease power dissipation by using PMOS cross-couple type with two sets of input terminals. Its oscillation frequency is dominated by the number of stage per row in series of differential amplifiers. Oscillation frequency decreases while the stage number increases. This design needs more chip area for more phases. The other twelve-phase coupled VCO [10] is composed of two coupled three-stage differential ring oscillators. The input NMOS transistors form the main oscillation path, and the PMOS transistors form the coupling path. The power consumption of such two coupled three-stage differential ring oscillators is lower compared with the conventional six-stage differential ring oscillator.

All previous works have the same problem: oscillation frequency decreases while the stage number increases. This work proposes new structure to solve this problem. The proposed new structure: differential ring oscillator with even stages is presented in the following section.

II. APPROACHES

To design a ring oscillator with differential delay cells, imitating a ring oscillator with interpolating scheme composed of inverters is a typical approach. Some of previous works use multiphase ring oscillator based on three-stage sub-feedback loops. It interchanges all the sub-feedback loops, and even number parts of output stages in main ring to avoid their oscillation conditions conflicting with each other. Such schemes reduce phase between adjacent sub-feedback loops, so the size of main ring should be larger than sub-feedback loops to avoid phase overlapping. If ring oscillator has multiphase and high oscillation frequency, the last stage or odd number parts of output stages in main ring must interchange, so oscillation condition conflicts should be resolved.

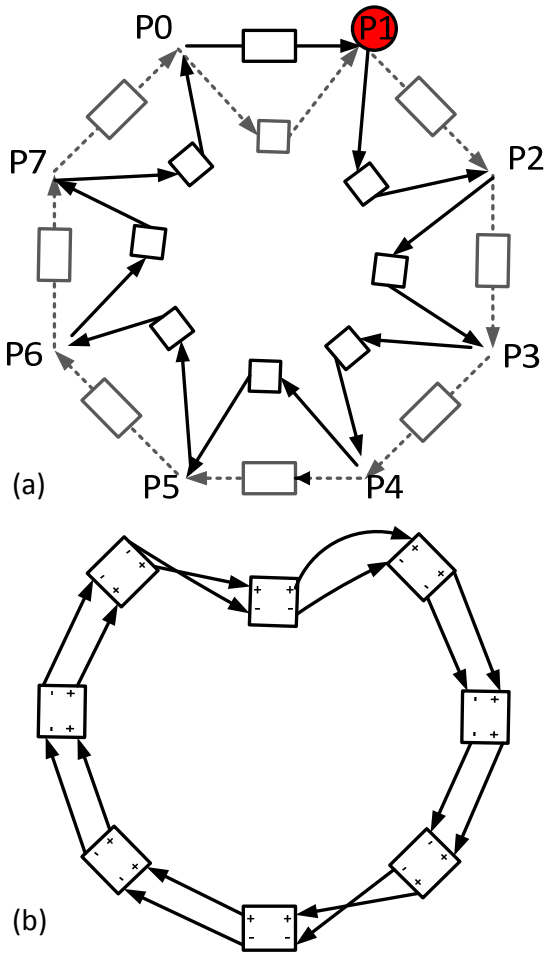

Figure 1. (b) is (a) dotted line path of sub-feedback loops without interchanging node.

To explain why the oscillation conditions have conflict , taking sixteen phases output ring oscillator with interpolating and cut set scheme for example as shown in Figure 1 and Figure 2. Ring oscillator in Figure 1 (a) and Figure 2 (a) interpolate at node P1 and all of their sub-feedback loops. They should get the same oscillation conditions. However, they get different results in numbers of interchanging parts. If ring oscillator produces uniform phases, every node should get the same oscillation condition. These phenomena don't happen in every sub-feedback loop. To resolve conflicts, the paths of sub-feedback loops can get different number of interchanging nodes. In Figure 3, a diagonally interpolating scheme in ring oscillator has four paths needed changes, because they have even number of interchanging nodes.

The interchanging output of sub-feedback loops, as shown in the dotted line in Figure 3, use the output interchanging scheme to unify the oscillation conditions. The relationships between interpolating scheme and interchanging node are show in Table 1. N means stages of main ring and k means stages of sub-feedback loops.

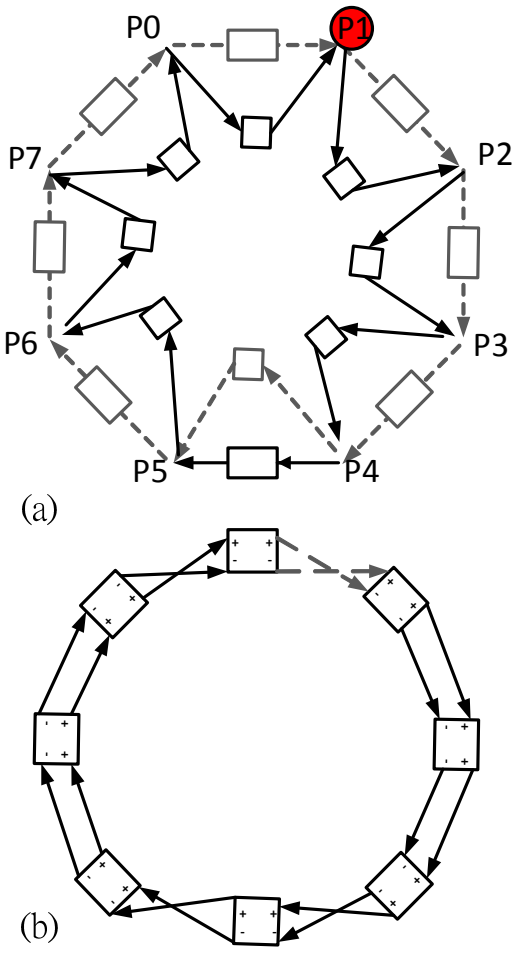

Figure 2. (b) is (a) dotted line path of sub-feedback loops with one interchanging node.

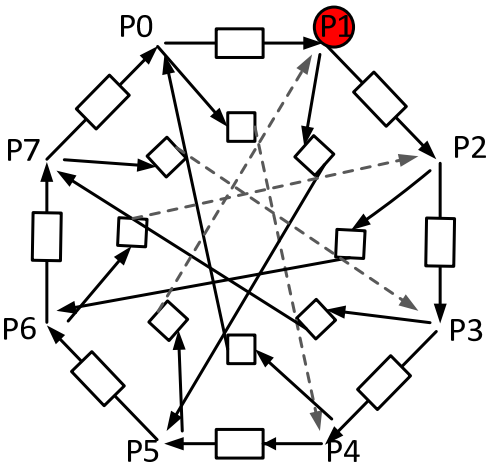

Figure 3. N=8 k=5 differential ring oscillator with diagonally interpolating scheme

To derive the relationship between oscillation frequency and phases, assuming its oscillation amplitude remains small and the waveform is sinusoidal-like, this work models the

signal path in the VCO with a first-order approximation [8] to confirm validity of such structure. Figure 4 shows a first-order approximation. gm, and Gm mean equivalent transduction of inverter in main ring, and equivalent transduction of inverter in sub-feedback loop, separately.

N	k	interchanging
8	2	7
8	3	6
8	4	5
8	5	4
8	6	3
8	7	2
8	8	1

Table 1. N=8 the relationship between k and number of interchanging nodes

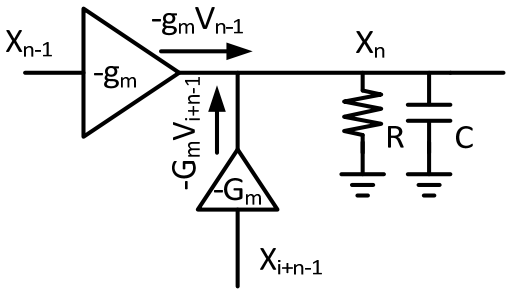

Figure 4. Combined single-stage equivalent circuit.

The first-order approximation can be describe by equation (1). Define θ as the phase difference between two adjacent nodes in main ring without interpolating scheme. In calculation, θ is total phase shift divided by total stages, and total phase shift is composed of dc phase shift and frequency-dependent phase shift. (e.g., θ=6π/5, for N=5) ∅ is phase difference between node X_n and X_{i+n-1}. Thus, the transfer model of a single stage can be found as equation (1), assuming all stages are the same.[8]

$$H(j\omega) = \frac{V_n}{V_{n-1}} = \frac{-g_m R}{(1+G_m R\cos\emptyset)+j(\omega RC - G_m R\sin\emptyset)} \quad (1)$$

According to the Barkhausen criterion of oscillation , the ring oscillator would oscillate if the loop has unity voltage gain and phase shift of 2π or multiple of 2π. Although there may exist some possible modes for long-chain ring, only those modes with enough loop gain can sustain oscillation. From equation (1), the minimum required gain of each stage can be written as

$$g_m R = \sqrt{(1+G_m R\cos\emptyset)^2 + (\omega_0 RC - G_m R\sin\emptyset)^2} = \frac{(1+G_m R\cos\emptyset)}{\cos\theta} \quad (2)$$

and the approximate oscillation frequency can be expressed as

$$\omega_0 = \frac{[G_m R\sin\emptyset + \tan\theta(1+G_m R\cos\emptyset)]}{RC} = \frac{\tan\theta}{RC} + \frac{k_0 G_m}{C} \quad (3)$$

$$k_0 = \sin[(i-1)\theta] + \tan\theta\cdot\cos[(i-1)\theta] \quad (4)$$

The first term of equation (3) is the oscillation frequency of a conventional ring oscillator. The second term corresponds to the frequency increment or decrement. Equation (3) actually overestimates the real oscillation frequency. However, this work is more interested in comparing the relative frequency improvement between different topologies using k_0 rather than calculating the absolute oscillation frequency.

k	θ	∅	k_0
3	202.5	135	0.4
4	202.5	157.5	0
5	202.5	90	1
6	202.5	157.5	0
7	202.5	135	0.4

Table 2. N=8 estimating $\theta, \emptyset \text{ and } k_0$ in different k

k	phase	frequency	Amplitude	m
2	16	1.26G	1.32mV	6
3	16	2.63G	1.26mV	6
4	16	773M	1.6mV	6
5	16	7.14G	400mV	6
6	16	810M	1mV	6
7	16	2.18G	1.5mV	6

Table 3. N=8 Hspice simulation results in different k

According to previous contents, in N=8 ring oscillator we can get θ as:

$$\theta = \frac{9\pi}{8} = 202.5^\circ$$

Because in new structure outputs of main ring and sub-feedback loops interchange in the same time, hand calculation of ∅ is complicated. Currently, we use the order of phase in Hspice simulation to get ∅. The results of estimates $\theta, \emptyset \text{ and } k_0$ are shown in table 2, and the results of simulation show in table 3. m=6 means size of sub-feedback loops are six times larger than size of main ring. We find that two results match, and even increase oscillation frequency with using diagonally interpolating technique.

This work :N=4, k=3 differential ring oscillator, as shown in figure 5-1.

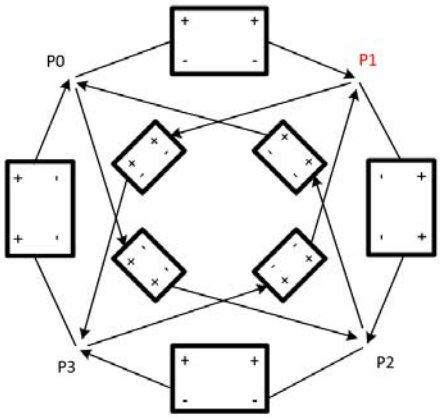

Figure 5-1. Structure of N=4, k=3

To promote the frequency of my structure, I merge the output load with a main ring delay cell and an sub feedback loops delay cell, as shown in figure 5-2, 5-3.

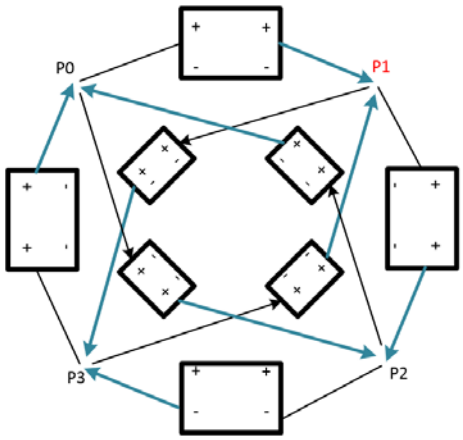

Figure 5-2. concept of merge the output load

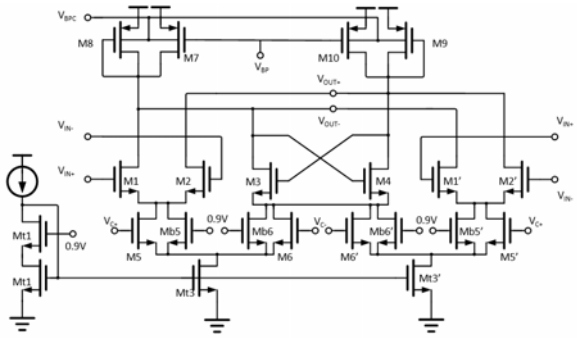

Figure 5-3. structure of merge the output load

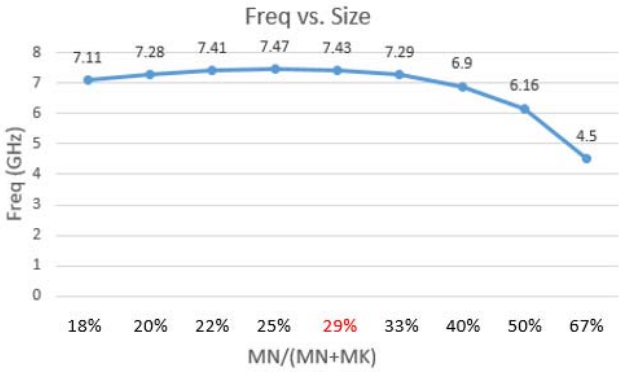

Table 4(a). N=4, k=3 the relationship between ratio of $M_N / (M_N + M_k)$ and oscillation frequency

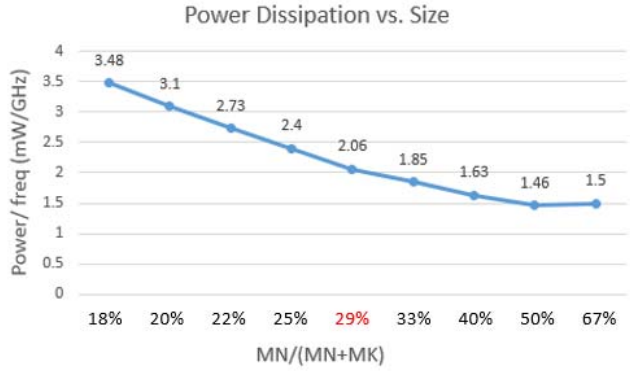

Table 4(b). N=4, k=3 the relationship between power/freq of $M_N / (M_N + M_k)$ and oscillation frequency

Because we use partial output interchanging scheme to avoid oscillation conditions conflicting and increase the phase between adjacent sub-feedback loops, the size of sub-feedback loops can be slightly larger than the size of main ring without phase overlap. Table 4 describes this situation. In the same power consumption, the highest oscillation frequency means optimization. $M_N / (M_N + M_k)$ is better to be designed in 25%~29%. M_N is the size of main ring. M_k is the size of sub-feedback loops.

Bulk−Controlled Process Compensator (BPC):
By constructing a negative feedback loop from bulk of gate-biased PMOS and diode−connected PMOS, compensate both PMOS simultaneously, as shown in figure 5-4, 5-5.

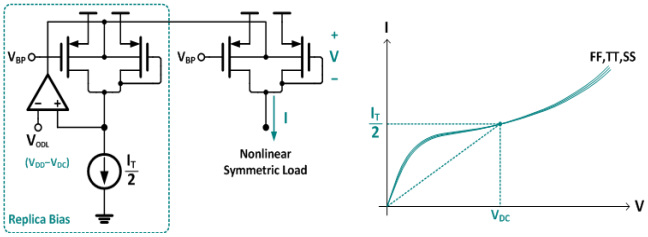

Figure 5-4. structure of BPC Compensator

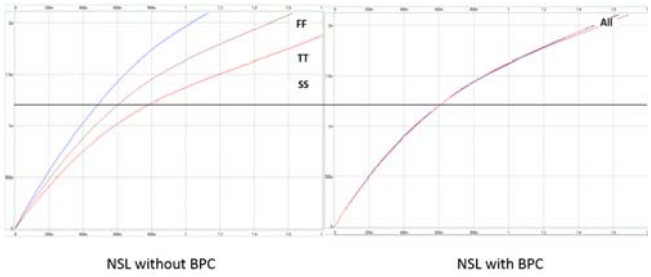

Figure 5-5. simulation of BPC Compensator(I-V curve)

Figure 6 shows PLL structure of this work. PLL is a negative feedback system that compares a feedback input phase with a reference input phase by Phase Frequency Detector (PFD), as shown in figure 7 and 8. Charge Pump (CP) and Common Mode Feedback (CMFB) transfer digital signal to analog signal, as shown in Figure 9 and 10, to control oscillation frequency of ring oscillator. Control Voltage Buffer (CVB) block control voltage and common mode feedback voltage, as shown in figure 11. Low Pass Filter (LPF) filter loop noise in PLL. Finally using divider to produce a feedback input signal to track a reference input signal until their phase difference is zero, as shown in figure12, 13. [7]

Considering the optimization between power consumption and oscillation frequency, this work finally uses N=4 k=3 ring oscillator to realize the design.

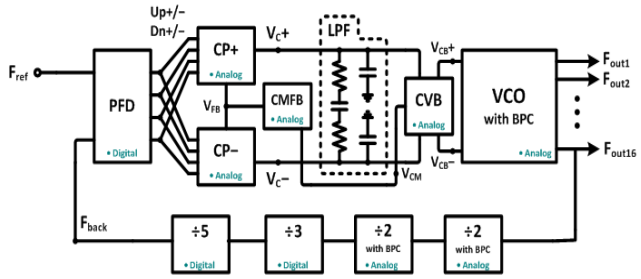

Figure 6. Structure of PLL

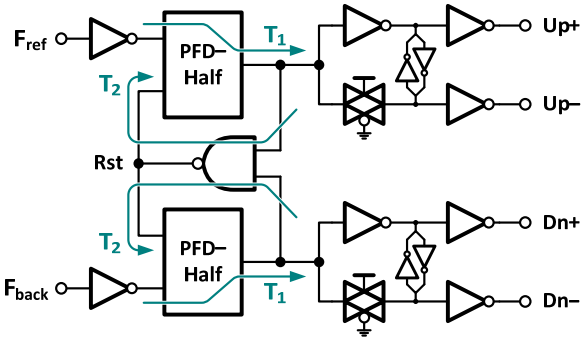

Figure 7. Structure of PFD

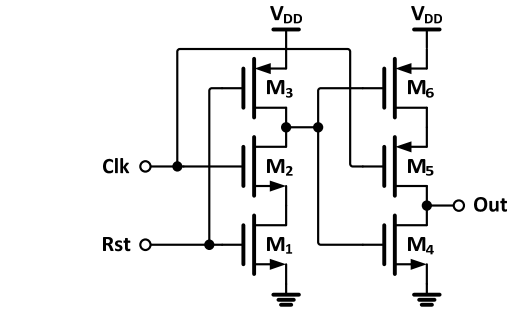

Figure 8. Structure of PFD-Half circuit

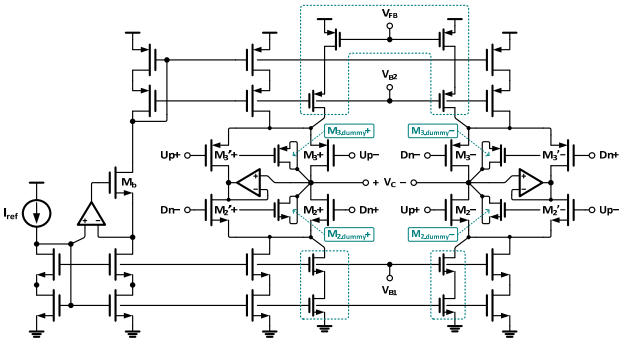

Figure 9. Structure of CP with CMFB

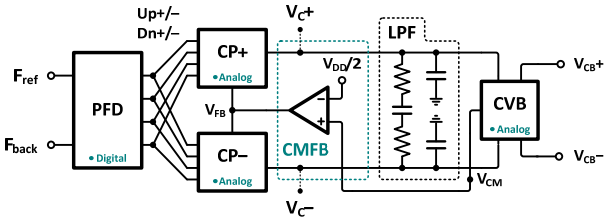

Figure 10. Structure of CMFB

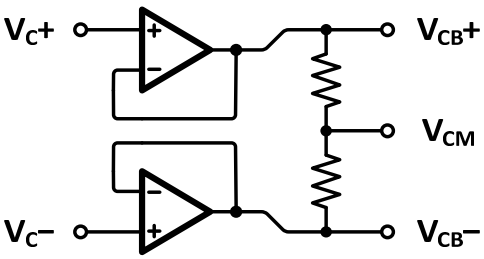

Figure 11. Structure of CVB

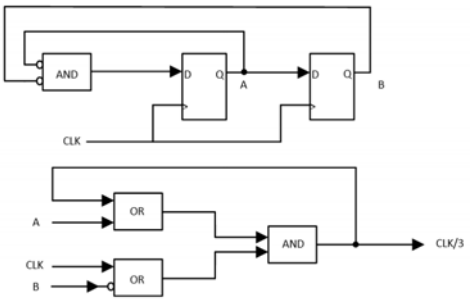

Figure 12. Structure of divider(divide by 3)

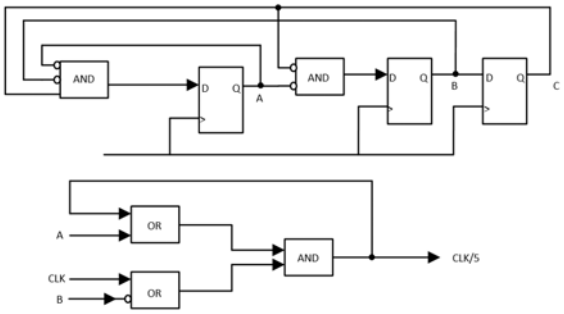

Figure 13. Structure of divider(divide by 5)

III. SUMMARY

7.5GHz and eight phases ring oscillator is achieved by optimizing a partial output interchanging scheme, using diagonally interpolating technique and using BPC scheme. All of specifications of this work perform in Table 6. It has better frequency performance comparing to previous work without inductance components as shown in Table 5(a), 5(b). This result overcomes the current 6-GHz frequency limitation of .18 um process, without using any inductance components to reduce chip area. The critical simulation result perform in Figure 14~16(b).

Reference	TCAS-I[23]	TCAS-II[9]	TVLSI[24]	JSSC[25]	TCAS-II[26]
Year	2009	2009	2009	2012	*2012
Technology(nm)	180	130	180	90	180
Supply Voltage(V)	1.8	1.2	1.8	1	1.8
Oscillation Frequency(GHz)	2.4	2.64	1.6	0.63~8.1	16.28
Total Power(mW)	36	31.2	17	7~26	10.8
*FOM	15	24.54	10.625	11.56	0.66

Reference	TVLSI[27]	TCAS-II[28]	JSSC[29]	[32]	This Work
Year	*2013	*2015	*2015	2015	2016
Technology(nm)	180	65	65	180	180
Supply Voltage(V)	1.8	1.2	1.2	1.8	1.8
Oscillation Frequency(GHz)	5.35	50.4~60.8	3.5	7	7.5
Total Power(mW)	8	30	21	58	50
*FOM	1.49	2.05	24.92	8.3	6.67

Table 5(a). summarizes ring oscillator design work published in IEEE in 2009~2015.

$$*\text{FOM} = \frac{\text{Power (mW)}}{\text{Freq (GHz)} \times \frac{\text{Tech (nm)}}{180} \times \frac{V_{DD}\text{ (V)}}{1.8}}$$

*(year) means this work uses inductance

Reference	TVLSI[27]	TCAS-II[28]	TCAS-II[9]	[32]	This Work
Year	*2013	*2015	2009	2015	2016
Technology(nm)	180	65	130	180	180
Supply Voltage(V)	1.8	1.2	1.2	1.8	1.8
Oscillation Frequency(GHz)	5.35	50.4~60.8	2.64	7	7.5
Phase Number(N)	4	8	12	8	8
Total Power(mW)	8	30	31.2	58	50
*FOM	0.373	0.256	2.045	1.038	0.834

Table 5(b). summarizes ring oscillator design work published in IEEE in 2009~2015 with comparison of phase number.

$$*\text{FOM} = \frac{\text{Power (mW)}}{\text{Freq (GHz)} \times \frac{\text{Tech (nm)}}{180} \times \frac{V_{DD}\text{ (V)}}{1.8} \times N}$$

*(year) means this work uses inductance

Technology(nm)	180
Supply Voltage	1.8
F_{ref}(MHz)	125
F_{out}(MHz)	7500
Divisor	60
K_{VCO}(MHz/V)	211
Total Power(mW)	50

Table 6. Specifications of this work

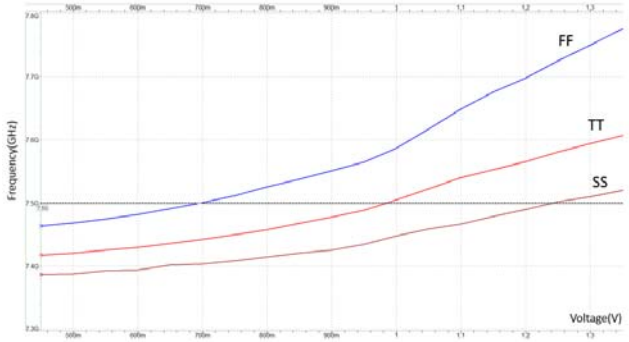

Figure 14. KVCO of ring oscillator in 0.45V~1.35V in this work

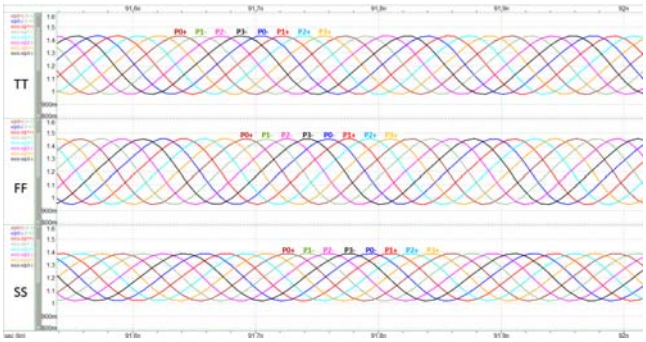

Figure 15 eight output phase of ring oscillator in this work

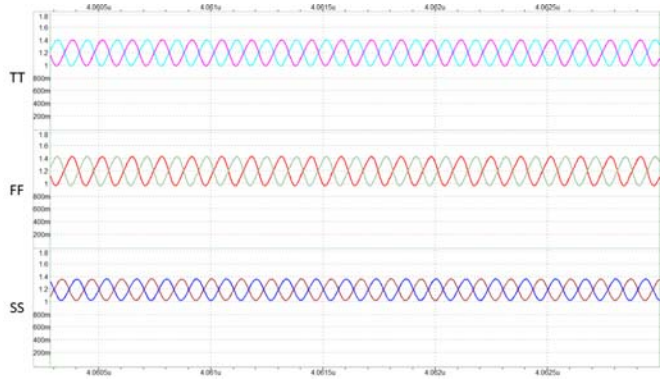

Figure 16(a) output signal (Vo) in PLL

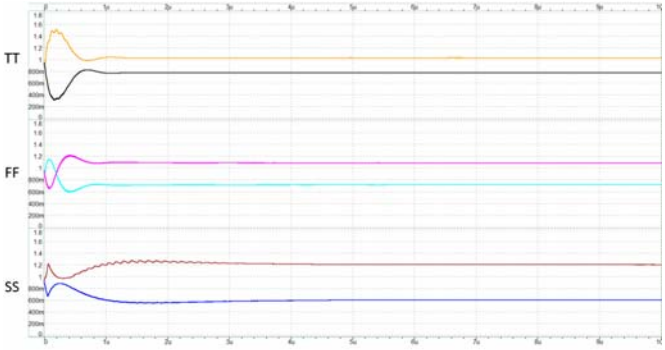

Figure 16(b) control voltage (Vc) in PLL

FUTURE WORK

This work emphasizes high oscillation frequency and multiphase of ring oscillator in PLL. It doesn't discuss about lowest power dissipation, locking time, variation of temperature, variation of supply voltage, etc. We could use different interpolating methods to solve previous problems in future.

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