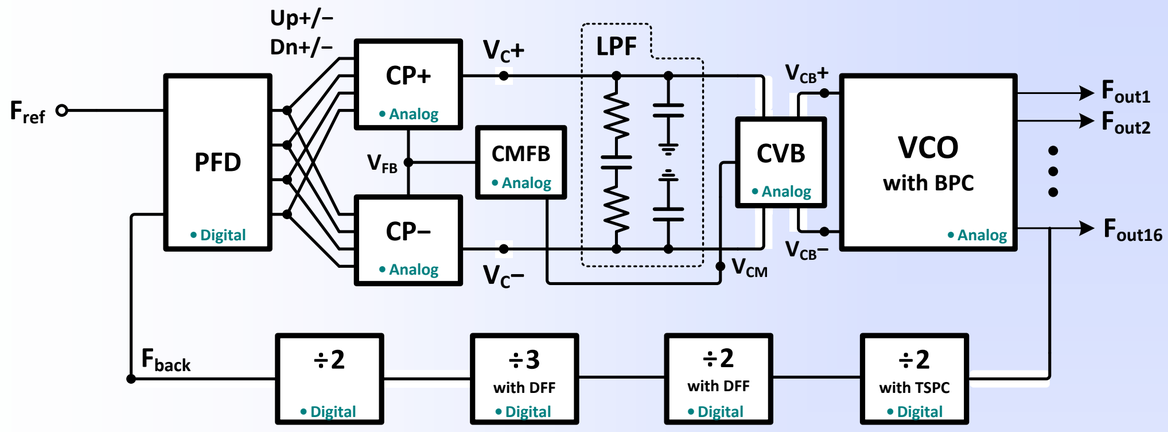
國立臺北大學電機工程學系103學年度專題報告海報

High frequency Multiphase Phase-Locked Loop

Nano Integrated Circuits and Systems Laboratory
Department of Electrical Engineering
National Taipei University
Teacher: Dr. Hong-Yi Huang
Student: Yu-Sian Yang

1. Introduction

- Phase-locked loop (PLL) is considered as tracking the input signal frequency and phase to change output clock and external reference clock in the same phase is called locked.
- A PLL with multiphase outputs is widely used in inter-IC synchronization such as DVD writing strategies and high-speed clock and data recovery circuits .
- Different kinds of Ring Oscillator composed by VCO for multiphase outputs :
  - 01. LC-Oscillator:
    a. Higher oscillator frequency
    b. Smaller modulation range, larger chip area, and is easy to be affect by different processes
  - 02. Single-ended Ring Oscillator:
    a. Great linearity, is easy to be designed
    b. Maximum operating frequency is inversely proportional to the unit delay element stages, only realized the odd stage output phase.
  - 03. Differential ring oscillator:
    a. Good anti-noise capability
    b. Frequency to voltage curve has poor linearity which cause larger jitter and phase error after it locked.
- For higher oscillator frequency, multiphase, lower power consumption, I choose differential ring oscillator in VCO.



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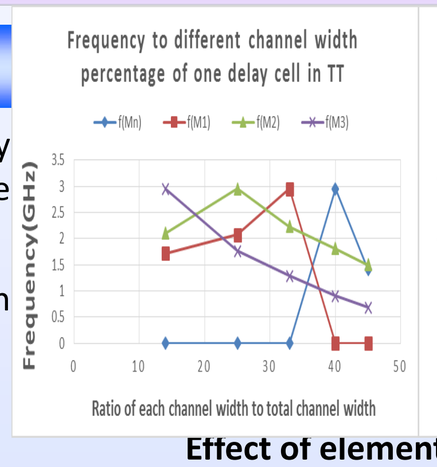
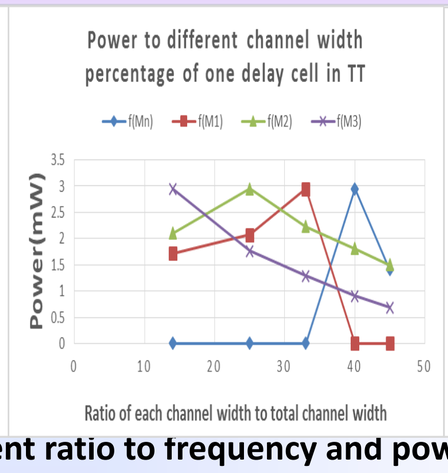
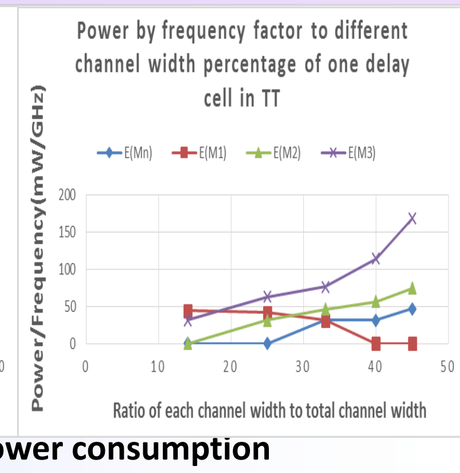
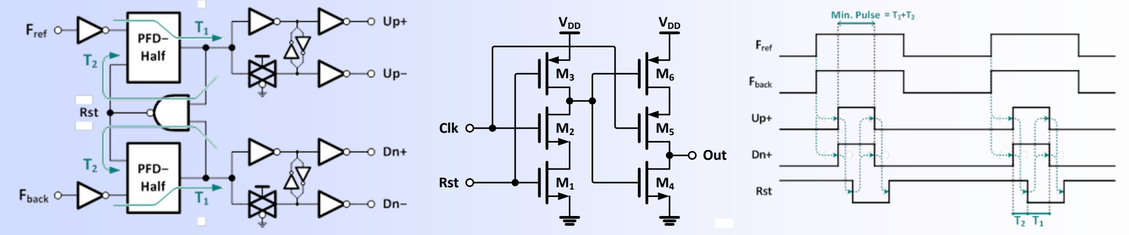




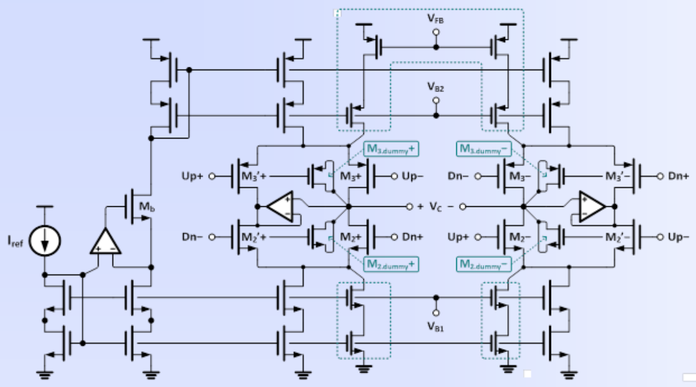


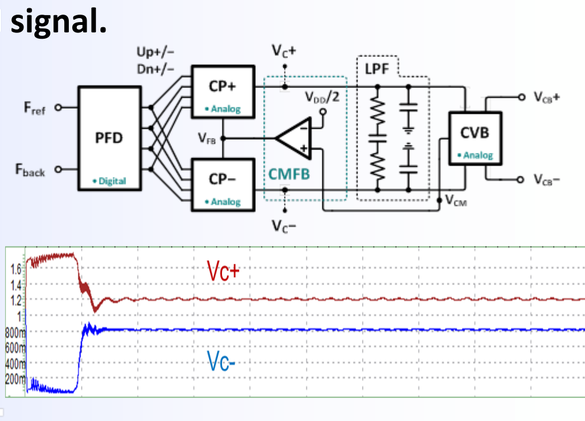
Effect of element ratio to frequency and power consumption

- 8-stage main ring delay cells.
- Larger Mn channel width percentage , lower the oscillation frequency .
- Larger Mn channel width is main to strengthen multiphase.
- Since the 2-stage sub-feedback loops shorten the signal feedback path, a higher oscillation frequency can be achieved by increasing Mn1 channel width percentage.
- An excess percentage of 2-stage sub feed-back loops for 8-stage main ring might cause the output signals being in the same phase.
- A larger Mn3 channel width percentage enhances the oscillation frequency .
- Finally, I choose Mn:M1:M2:M3=4:3:2:1, this is the best ratio I find.



Phase Frequency Detector (PFD) : Compares Fref and Fback to produce UP and DN signal.

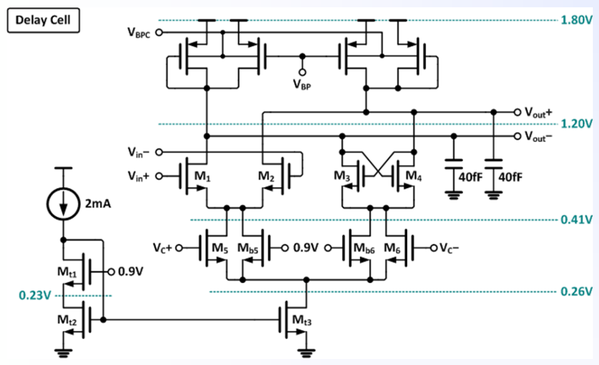




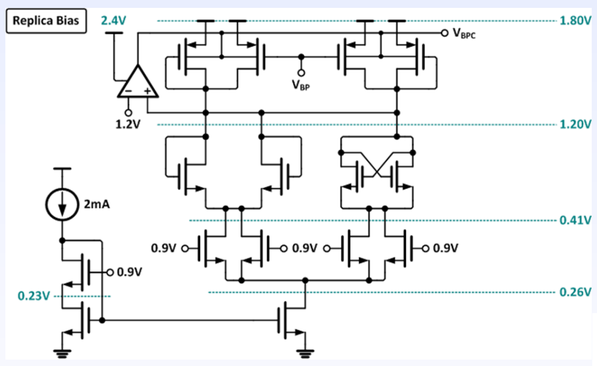
TDC test time-output code relationship and simulation of time to digital code

2. Theoretical Analysis

- Delay element of VCO with bulk−Controlled input Port :



- Replica Bias Circuit for BPC Technique to Compensate VCO:



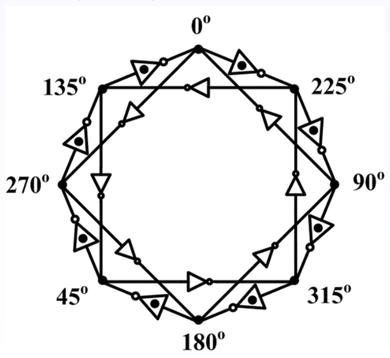
- In a stable ring oscillator, there should only be one possible phase that can exist in one output node in which every output node must be oscillating in phase.

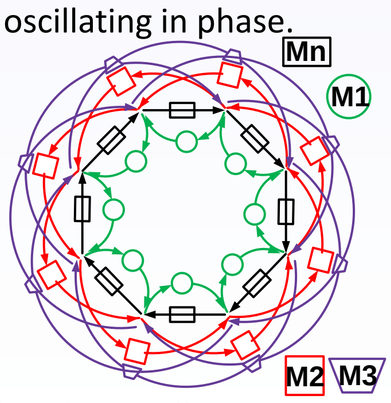
ex: N=3p+2

$$\theta = (240^o - \frac{120^o}{N})$$

$$Ex: N = 8$$

$$\theta = (240^o - \frac{120^o}{8}) = 225^o$$





My ring oscillator structure

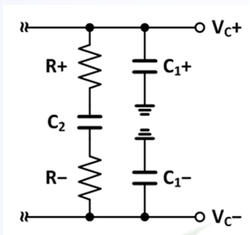
3. Conclusion

Advantage :

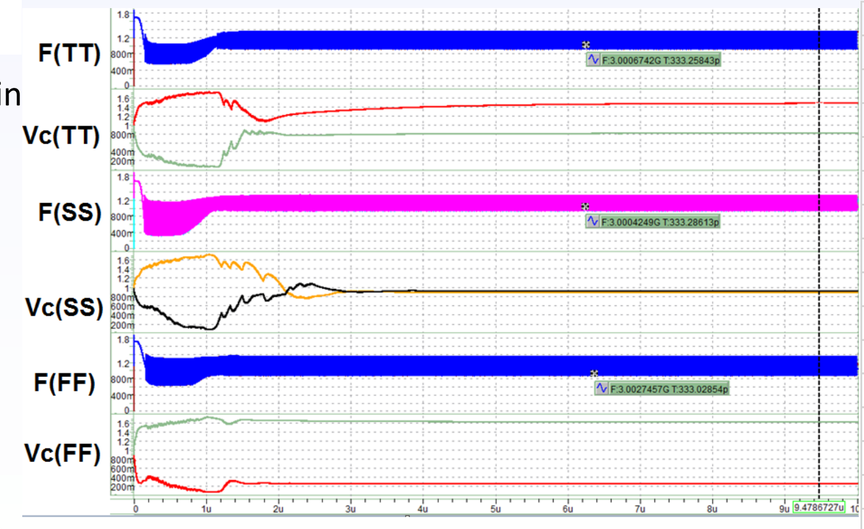
- The process less affect the frequency of high frequency multiphase phase locked loop.

Disadvantage :

- Lower maximum frequency
- Higher power dissipation



	F(TT)	F(SS)	F(FF)	Power	Phase(N)	P/(F*N) (MW/GHz)
previous work	5G	4.38G	4.93G	38.8mW	12	0.499
my work	3G	3G	3G	92mW	16	1.9



Spec of the PLL	
Process	0.18um
Power supply	1.8V
Fref	125M
Fout	3G
Divisor	24
Kvco	1244MHz/V
Locking Time	2us
R+,R-	27279.8
C1+,C1-	1.09pF
C2	4.35pF
Cp current	10uA
Phase margin	53.1
Unity Gain Freq	2MHz
Power Dissipation	92mW
Jitter	53