分數型頻率除頻器

Frational Frequency Divider

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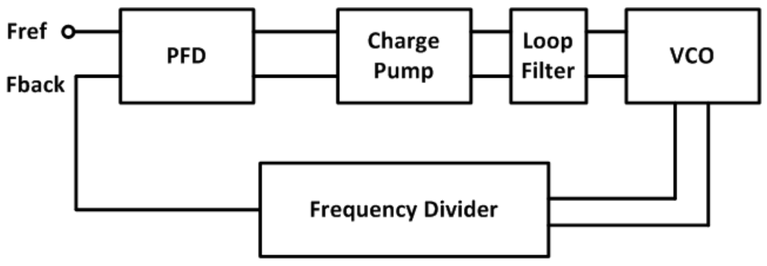
Related Technology

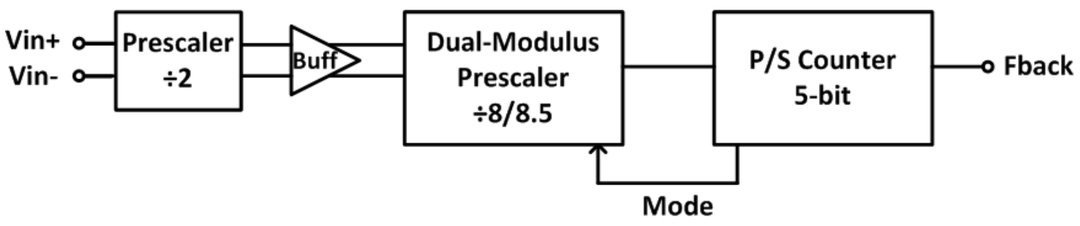


- Frequency Divider is used in PLL (Phase-Locked Loops)
- According to 802.11a, channel spacing = 20 MHz.

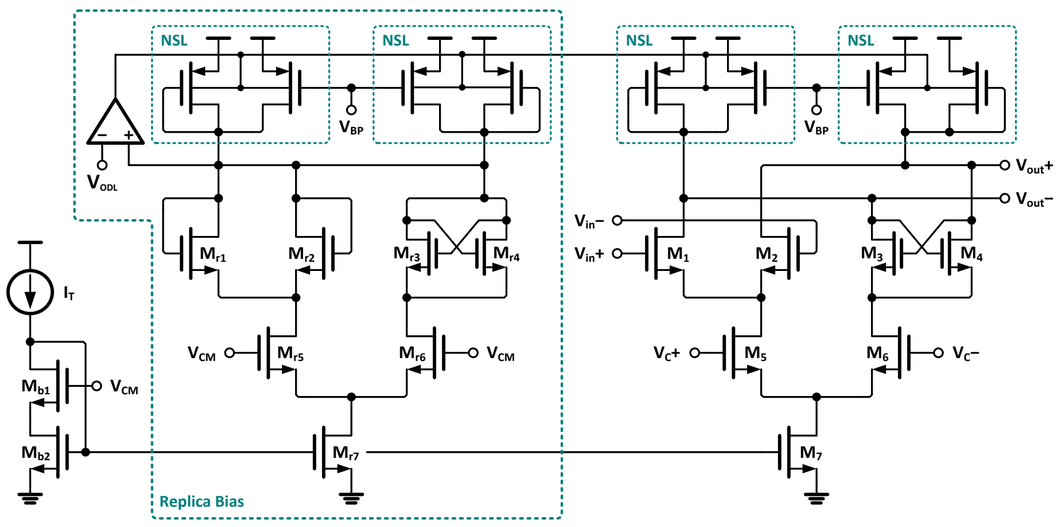
Motivation

- Try to design a decimal point to have closer operating frequency steps.
- Try to improve this work by decreasing the power dissipation, needed IC area.

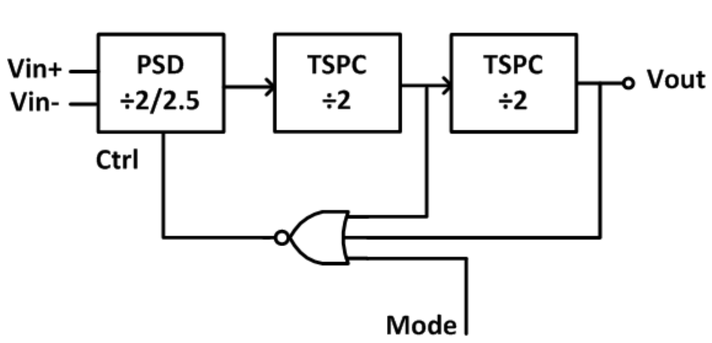
Circuit Design

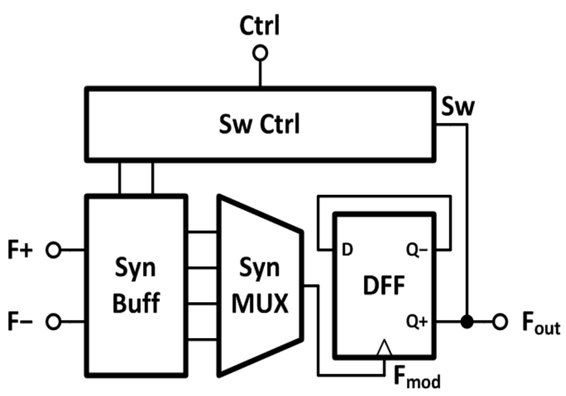


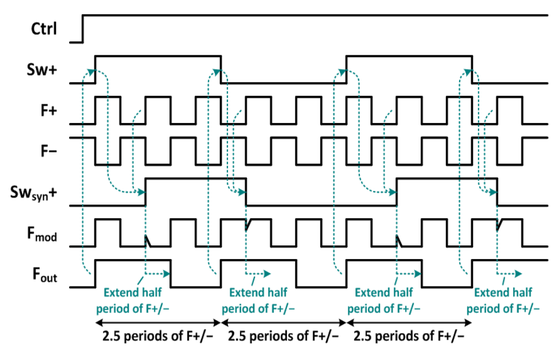
Differential High Speed Divider



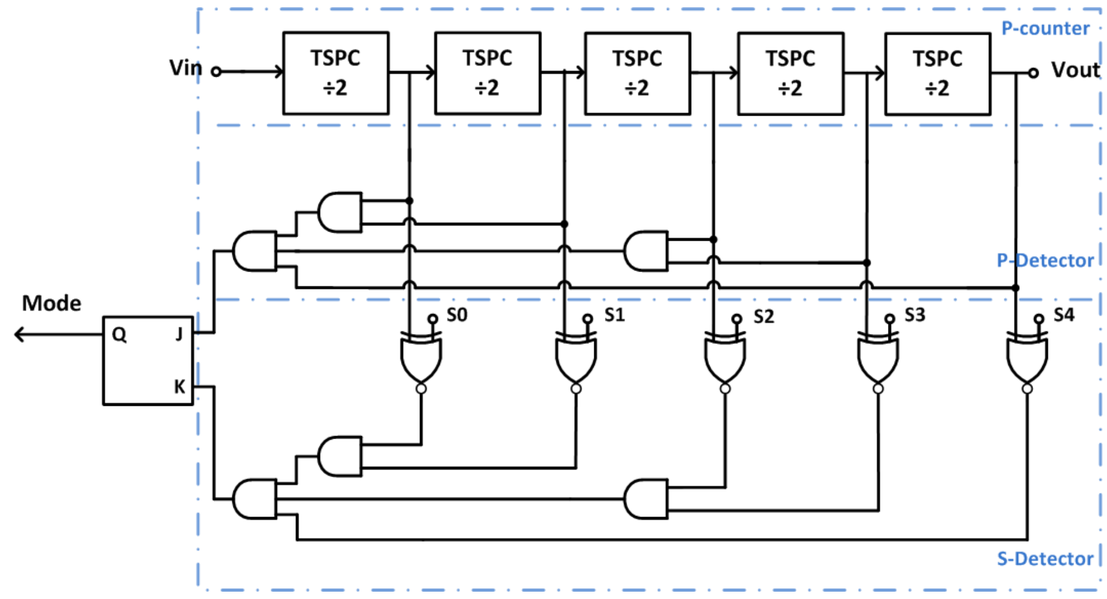
Dual-Modulus Prescaler & PSD



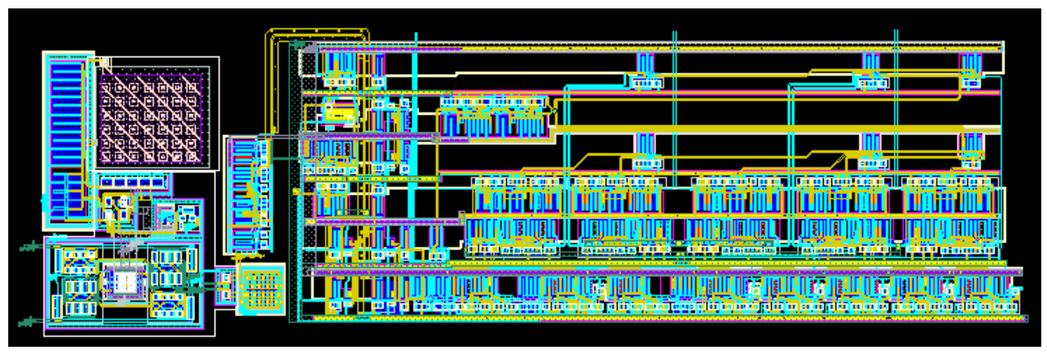




P-counter & P/S Detecter



Simulation & Layout



Comparison

- **Power Consumption**

	Divider	Buffer	Total
Original Work	4.8mW	2.9mW	7.7mW
This Work	6.16mW*	1.64mW	7.8mW

*Divider(6.16mW)=prescaler(1.93mW)+counter(4.23mW)

- **Performance**

	Operating Frequency	VCO Frequency Steps	Division Ratio	Fref
Original Work	5.14~5.36 GHz 5.72~5.86 GHz	20 MHz	514~536 572~586	10 MHz
This Work	5.13~5.43 GHz	10 MHz	513~543	10 MHz

Conclusion

By Using Phase Switch Divider with TSPC Structure

- Create a smaller division ratio’s step of Frequency Divider.
- Operating in Higher Frequency.

By Using D Flip-Flops in Counter

- Perfect align the signal delivered to P-counter and S-counter.
- Brings more power consumption and layout area.