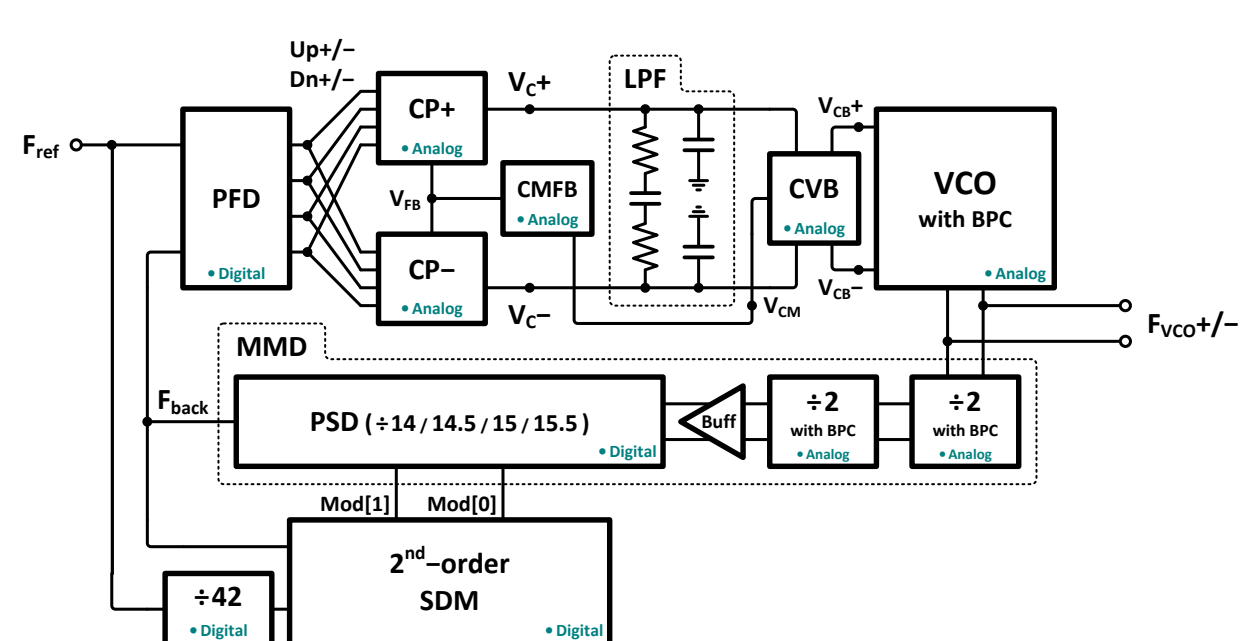


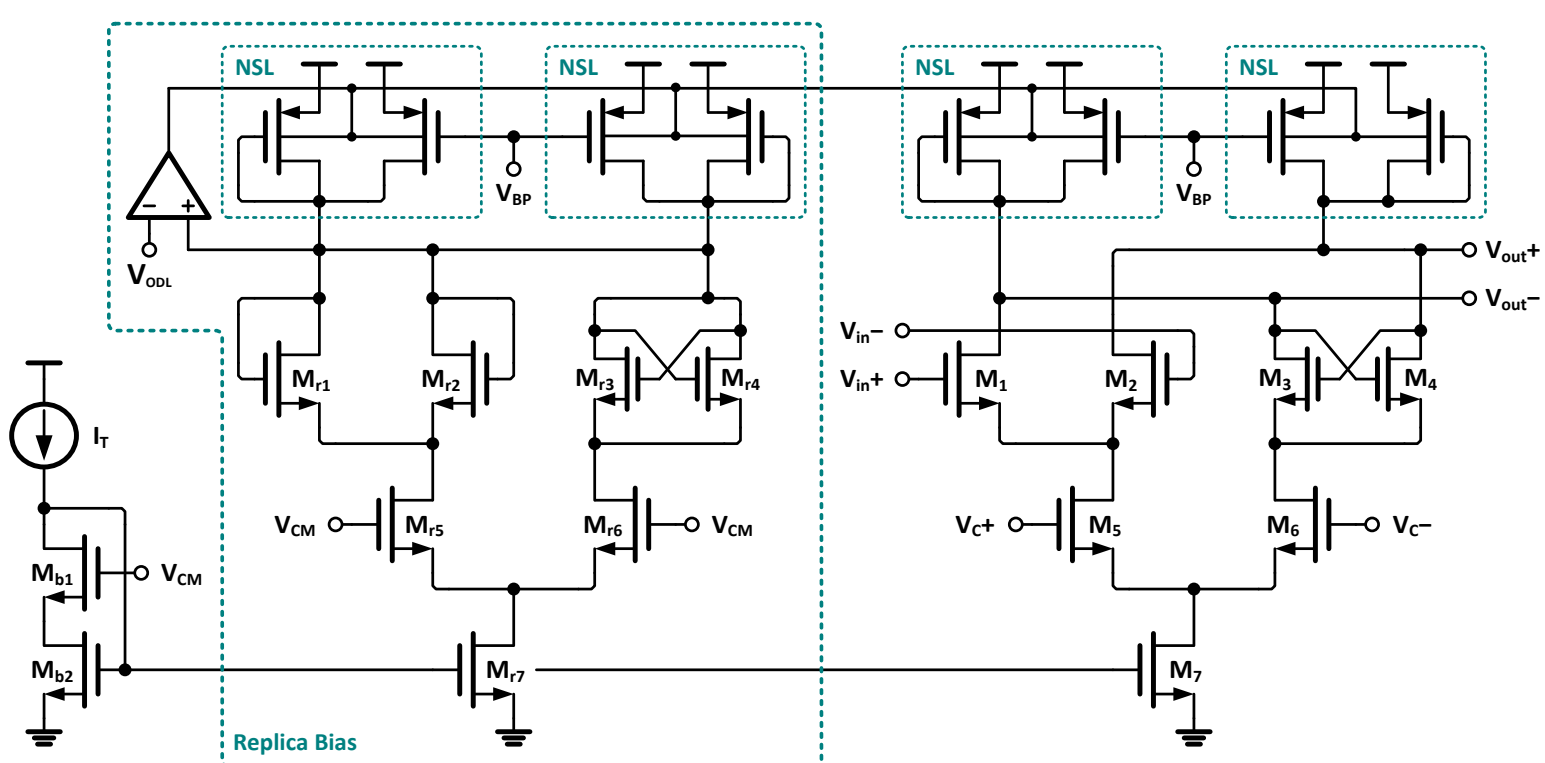
### Research Target

- Complete design of SATA III SSCG
- Use process compensation technique for VCO, high speed divider in order to reduce power dissipation.
- Compensate the modulus chasm of MMD and let SSCG to achieve the specification of SATA III. Use 2nd-Order Sigma-Delta Modulator to achieve high EMI reduction with triangular profile.
- Improve this work by decreasing the power dissipation, needed IC area and the performance of Sigma-Delta Modulator.
- Complete layout of VCO and high-speed divider with BPC technique.

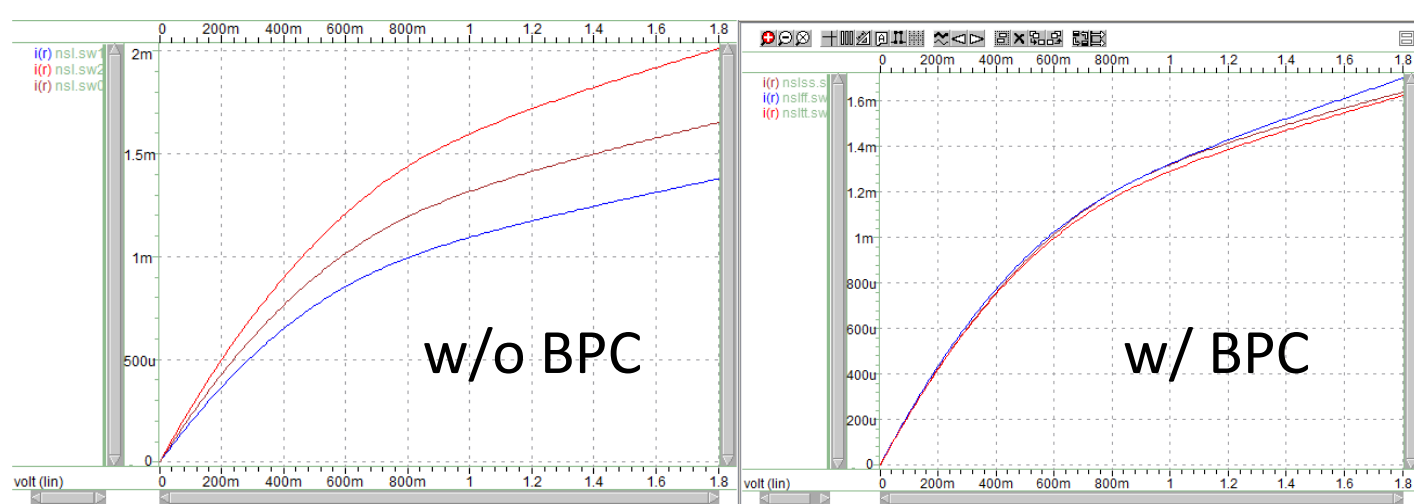
### Introduction of Circuit Structure



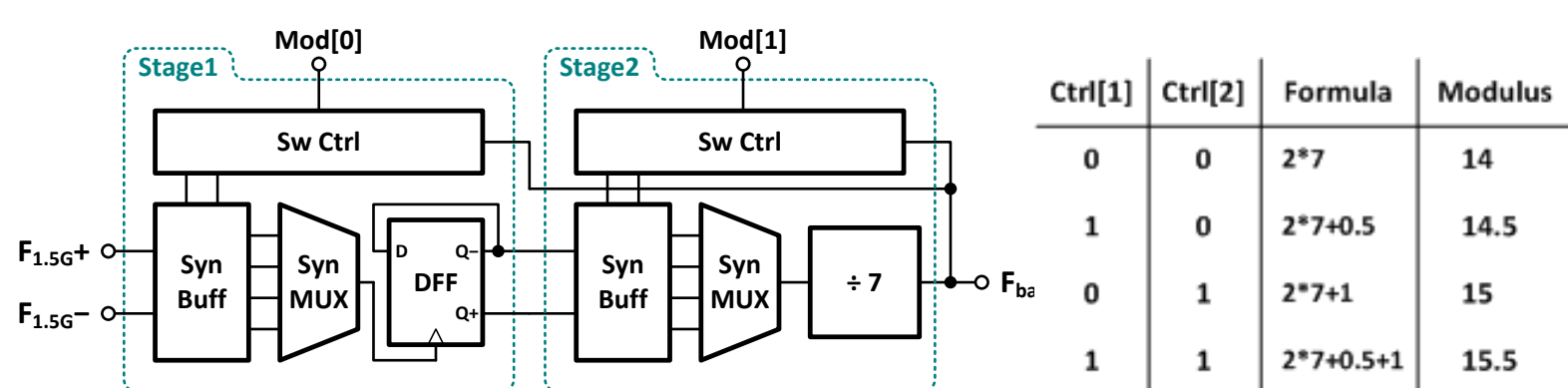
### SATA III Spread Spectrum Clock Generator



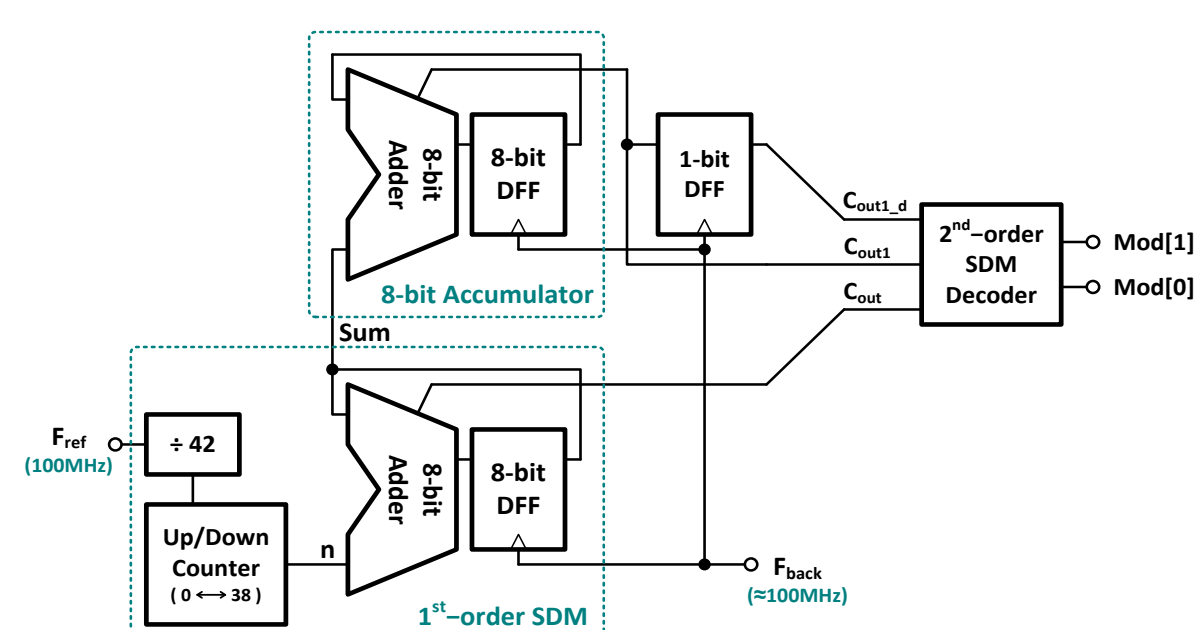
### Voltage-Controlled Oscillator with BPC Technique



### Simulation Of NSL

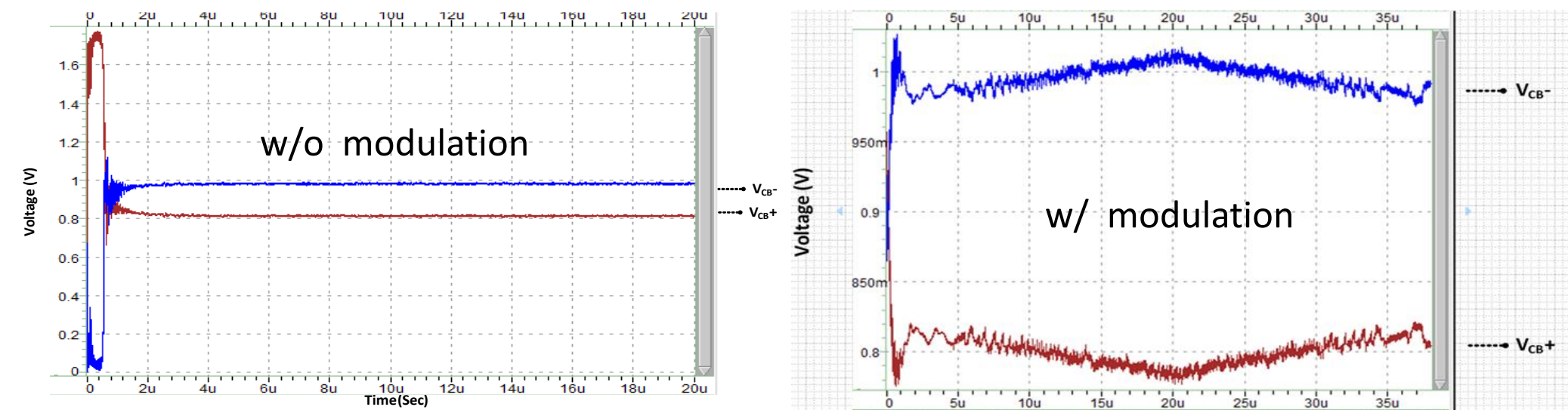


### ALL Modulus Phase Switch Divider

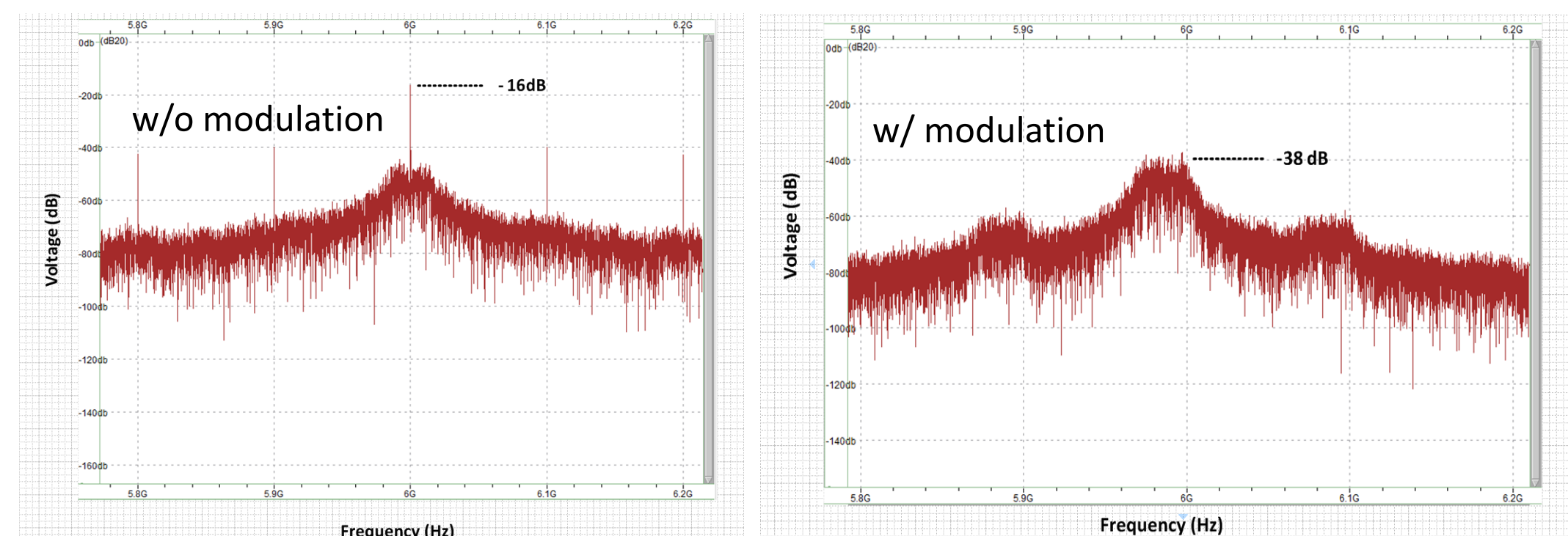


### Schematic Of SATA III 2nd-order SDM

### Experimental Results

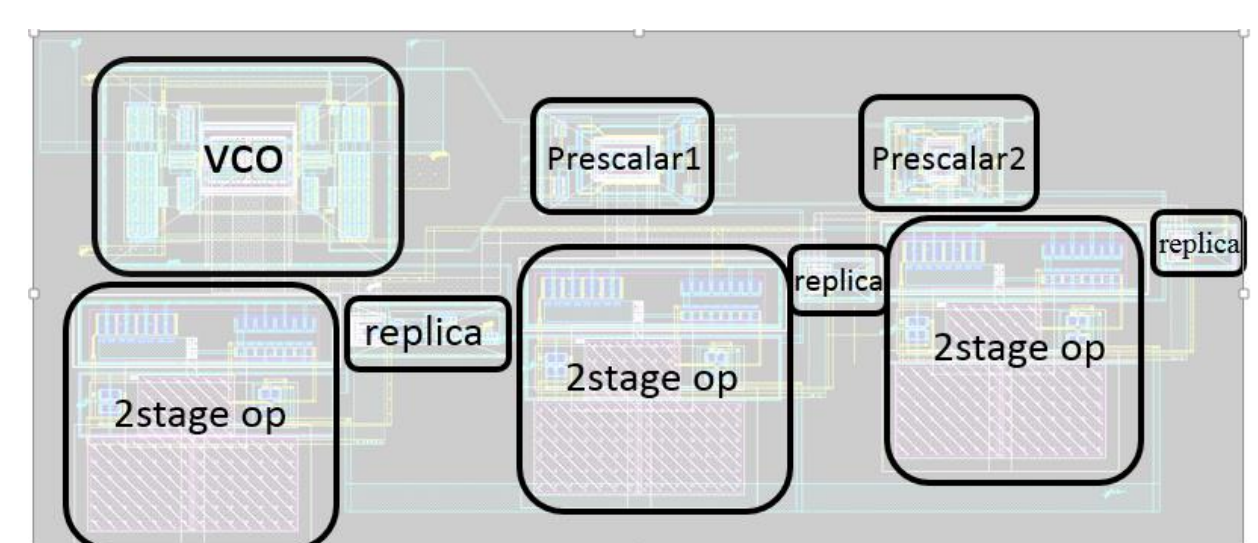
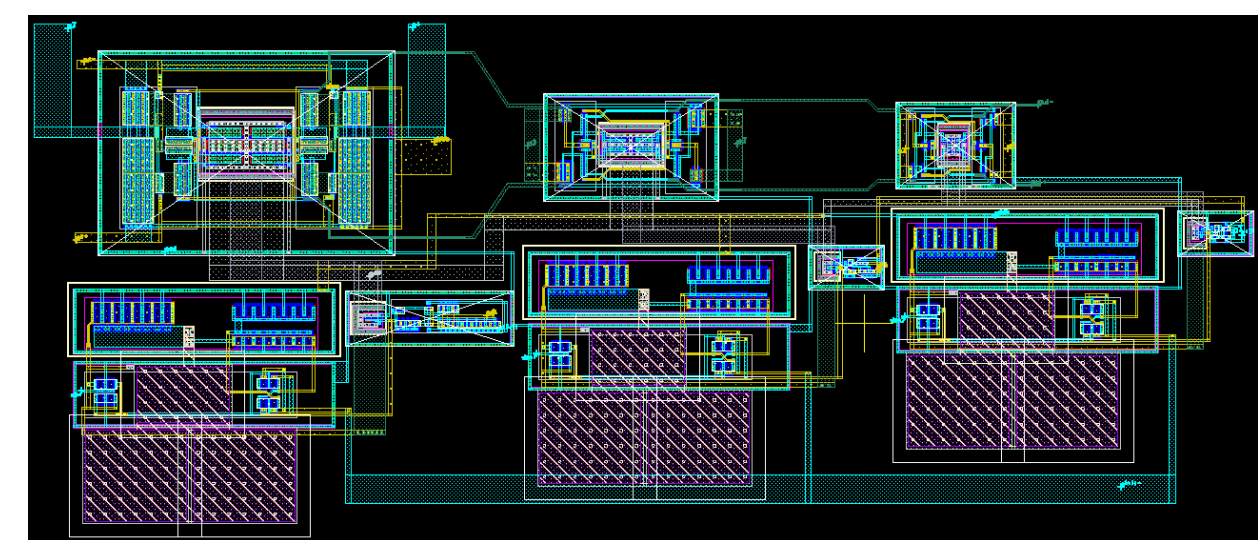


### The control voltage of VCO w/o and w/ modulation



### The spectrum of SSCG w/o and w/ modulation

### Layout of VCO and high-speed divider(with BPC):



### Conclusion

- By Using Bulk-Controlled Process Compensator Technique :
  - a. Output frequency of VCO can be nearly independent to process variation.
  - b. Optimum Division Operation of prescaler could be achieved.
  - c. Chip yield could be improved by BPC scheme.
  - d. Less current is needed and so power consumption is decreased.
  - e. With lower KVCO, smaller capacitor used in low pass filter is needed.
- By using all Modulus Phase Switch Divider :
  - Cancel the modulus chasm of MMD and succeed SATA III specification.
- By using 2<sup>nd</sup>-order Sigma-Delta Modulator :
  - Achieve High EMI Reduction with Triangular profile.

### Power Dissipation Comparison :

	VCO +Calibration	Divider	PFD/CP	Other	Total
JSSC[13]	13mW	31mW	3mW	-	47mW
This Work	7.74mW	5.016mW	683.7uW	4.45mW	17.889mW

\*5.01mW=1.404mW(1<sup>st</sup> Prescaler) + 0.225mW(2<sup>nd</sup> Prescaler) + 3.387mW(Buffer&PSD)